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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Scott Fink et al.

Serial No.: 09/522,026

Filed: October 8, 1998

For: A Microcontroller Having an N-Bit Data Bus Width with Less than N I/O Pins and Method Therefor

§ Group Art Unit: 2508

§ Examiner: R. Potter

§ Atty Docket: M71462USD1

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July 24, 2000 Kerry Morris
Signature

Office of the Deputy Assistant
Commissioner for Patent Policy and Projects
Washington, D.C. 20231

Dear Sir:

PRELIMINARY AMENDMENT

Applicants hereby submit a Preliminary Amendment for the above-identified patent application. Applicants respectfully request that the amendments set forth below be entered before prosecution on the merits.

AMENDMENT

In the Claims:

Please cancel claims 1-10 and add the following new claims:

-- 11. A method of operating a microcontroller in an integrated circuit package (IC), said method comprising the steps of:

providing an IC chip with a microcontroller having a data bus;

providing a first pin electrically coupled to said microcontroller, wherein said first pin functions as a power supply pin;

providing a second pin electrically coupled to said microcontroller, wherein said second pin functions as a grounding pin; and

providing a plurality of third pins electrically coupled to said microcontroller, wherein said plurality of third pins are function pins, at least one of said plurality of third pins being a multiple function pin, whereby a total number of said first, second and plurality of third pins is at least three which is less than or equal to a bit bus width of said data bus.

12. The method of claim 11, wherein each of said plurality of third pins are one of input only pins or input/output pins.

13. The method of claim 11, further comprising the step of providing at least one configuration circuit coupled to each of said plurality of third pins and to said data bus for determining a function for a corresponding one of said plurality of third pins.

14. The method of claim 13, wherein the step of determining a function for a corresponding one of said plurality of third pins comprises the step of enabling only one at a time of said at least one configuration circuits for each of said plurality of third pins so as to configure a corresponding one of said plurality of third pins to a function associated with said enabled one of said at least one configuration circuits.

15. The method of claim 13, further comprising the step of coupling independent function lines to each of said configuration circuits and to a corresponding one of said plurality

of third pins for transferring data between said corresponding one of said plurality of third pins and said microcontroller when a particular one of said configuration circuits is enabled.

16. The method of claim 15, further comprising the step of coupling a signal bus to said control register and to said microcontroller for sending signals from said microcontroller to said control register on which of said configuration circuits need to be enabled and which of said configure circuits need to be disabled.

17. The method of claim 13, further comprising the step of coupling a control register to said data bus for enabling and disabling each of said configuration circuits for determining a function for each of said plurality of third pins.

18. The method of claim 17, further comprising the step of coupling control signal lines to said data bus and to each of said configuration circuits for transferring to each of said configuration circuits one of said enable and disable signals.

19. The method of claim 17, wherein said control register is adapted to hold a known logic state.

20. The method of claim 17, wherein said control register is a memory device.

21. A method of operating a microcontroller in an integrated circuit package (IC), said method comprising the steps of:

providing an IC chip with a microcontroller having a data bus;

providing a first pin electrically coupled to said microcontroller, wherein said first pin functions as a power supply pin;

providing a second pin electrically coupled to said microcontroller, wherein said second pin functions as a grounding pin;

providing a plurality of third pins electrically coupled to said microcontroller, wherein said plurality of third pins are function pins, at least one of said plurality of third pins being a multiple function pin, whereby a total number of said first, second and plurality of third pins is at least three which is less than or equal to a bit bus width of said data bus;

providing at least one configuration circuit coupled to each of said plurality of third pins and to said data bus for determining a function for a corresponding one of said plurality of third pins, wherein only one of said at least one configuration circuit for each of said plurality of third pins is enabled at a time to configure a corresponding one of said plurality of third pins to a function associated with said one of said at least one configuration circuit which is enabled;

coupling independent function lines to each of said configuration circuits and to a corresponding one of said plurality of third pins for transferring data between said corresponding one of said plurality of third pins and said microcontroller when a particular one of said configuration circuits is enabled;

coupling a control register to said data bus for enabling and disabling each of said configuration circuits for determining a function for each of said plurality of third pins;

coupling control signal lines to said data bus and to each of said configuration circuits for transferring to each of said configuration circuits one of said enable and disable signals; and

coupling a signal bus to said control register and to said microcontroller for sending signals from said microcontroller to said control register on which of said configuration circuits need to be enabled and which of said configure circuits need to be disabled.

22. The method of claim 21, wherein each of said plurality of third pins are one of input only pins or input/output pins.

23. The method of claim 21, wherein said control register is adapted to hold a known logic state.

24. The method of claim 21, wherein said control register is a memory device.--

Applicants respectfully request that the amendments below be entered and submit that these amendments will put the claims in condition for allowance, or in better form for appeal. No new matter has been entered. Antecedent basis for the amendments may be found throughout the specification and drawings as originally filed.

Applicants request reconsideration in light of the amendments and remarks contained herein.

Respectfully submitted,

DATE: July 24, 2000

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